FIG.1

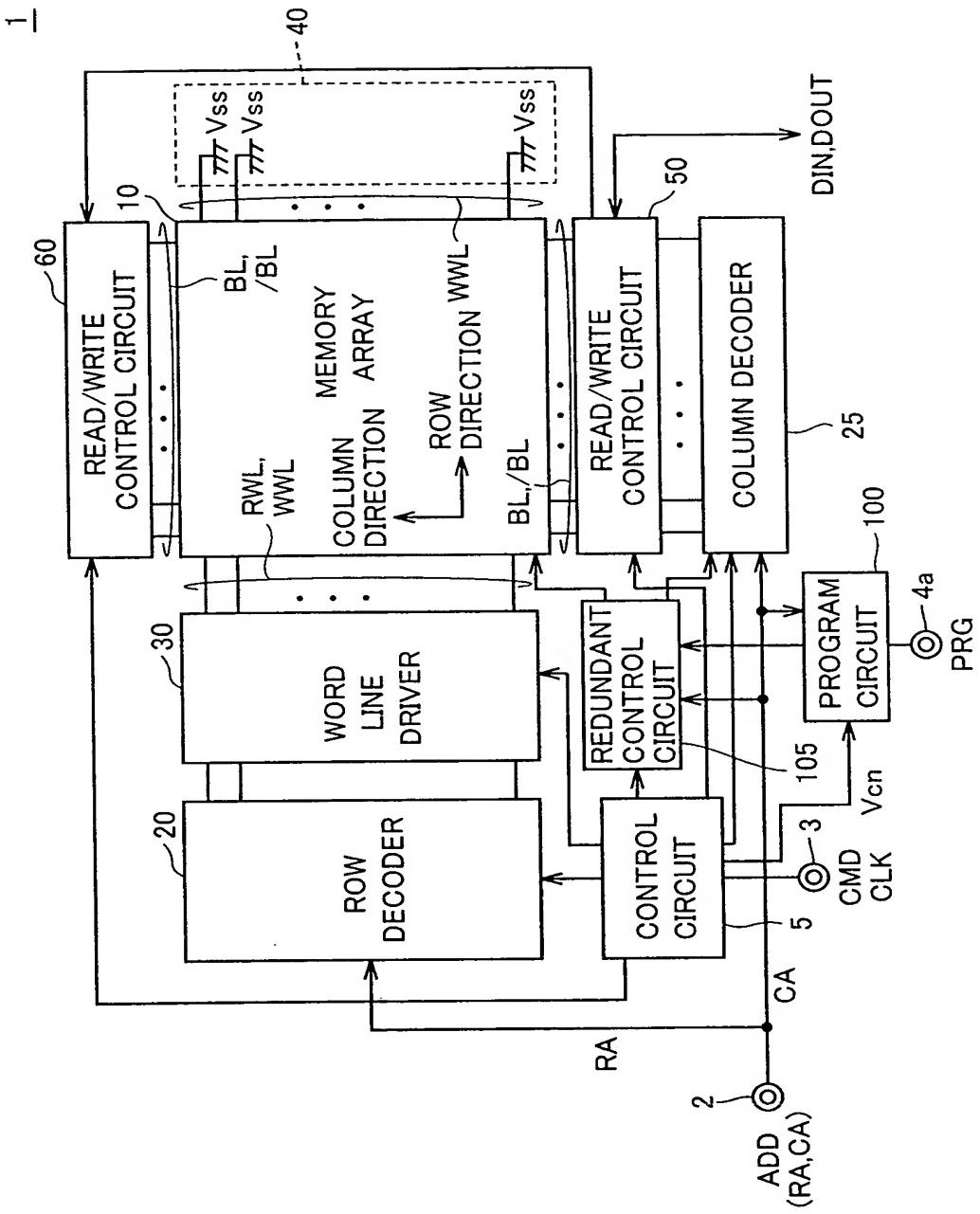

1
40
Vss
Vss
Vss
10
60
READ/WRITE CONTROL CIRCUIT
BL, /BL
MEMORY ARRAY
ROW DIRECTION
WWL
RWL, WWL
COLUMN DIRECTION
BL, /BL
50
READ/WRITE CONTROL CIRCUIT
DIN,DOUT
COLUMN DECODER
25
100
PROGRAM CIRCUIT
4a
PRG
30
WORD LINE DRIVER
REDUNDANT CONTROL CIRCUIT
105
Vcn
20
ROW DECODER
CONTROL CIRCUIT
3
CMD CLK
5
CA
RA
2
ADD (RA,CA)

FIG.2

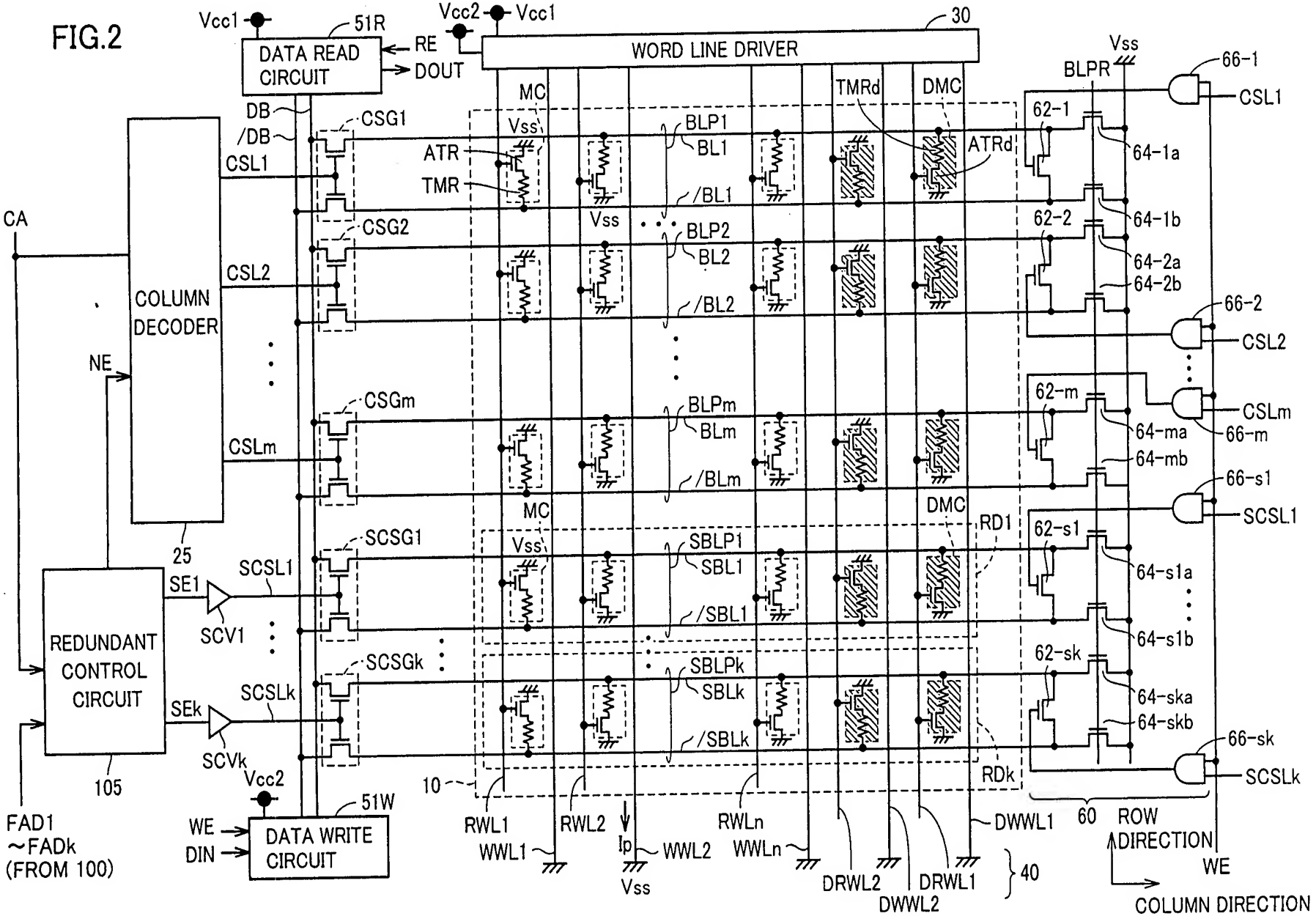

Vcc1
51R
DATA READ CIRCUIT
RE
DOUT
Vcc2
Vcc1
WORD LINE DRIVER
30
Vss
BLPR
66-1
CSL1
MC
TMRd
DMC
DB
/DB
CSG1
Vss
BLP1
BL1
/BL1
ATR
TMR
ATRd
62-1
64-1a
CA
CSG2
Vss
BLP2
BL2
/BL2
62-2
64-1b
64-2a
64-2b
66-2
CSL2
CSL1
COLUMN DECODER
CSLm
CSGm
BLPm
BLm
/BLm
62-m
64-ma
64-mb
CSLm
66-m
NE
MC
DMC
RD1
66-s1
SCSL1
SCSG1
Vss
SBLP1
SBL1
/SBL1
62-s1
64-s1a
64-s1b
25
SE1
SCSL1
SCV1
SCSGk
SBLPk
SBLk
/SBLk
62-sk
64-ska
64-skb
66-sk
SCSLk
REDUNDANT CONTROL CIRCUIT
SEk
SCVk
105
Vcc2
10
RDk
51W
DATA WRITE CIRCUIT
WE
DIN
FAD1
~FADk
(FROM 100)
RWL1
WWL1
RWL2
Ip
WWL2
Vss
RWLn
WWLn
DRWL2
DRWL1
DWWL2
DWWL1
40
60
ROW DIRECTION
WE
COLUMN DIRECTION

FIG.3

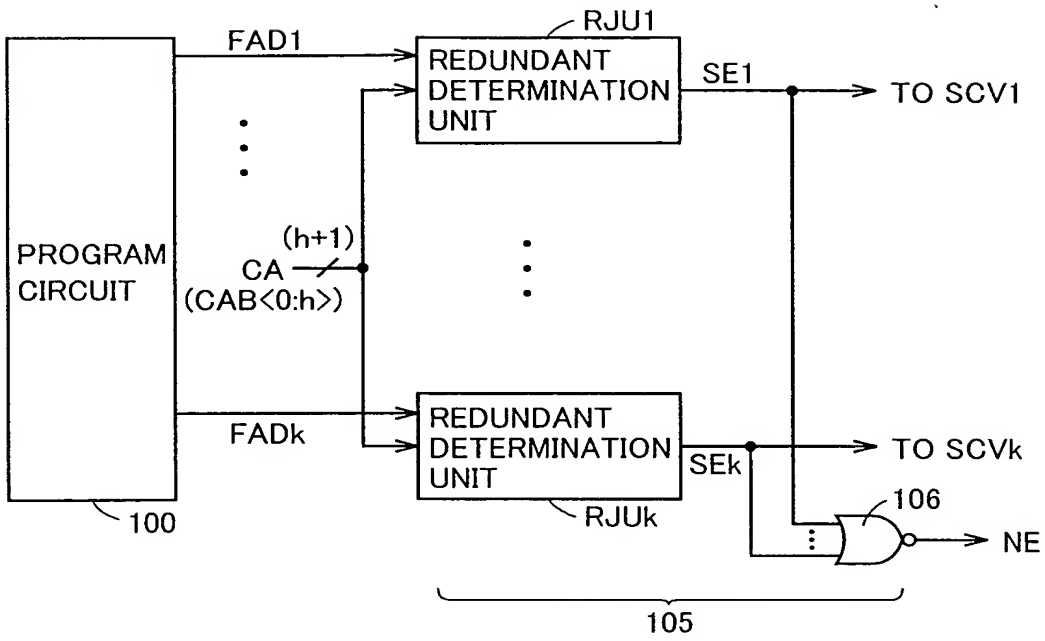
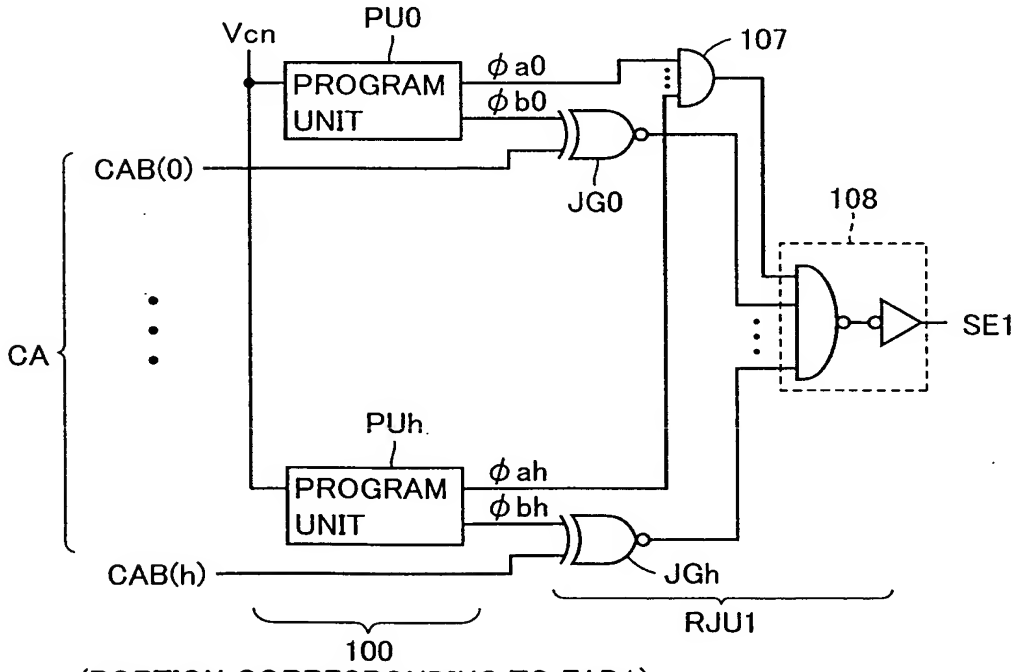


FIG.4



(PORTION CORRESPONDING TO FAD1)

FIG.5

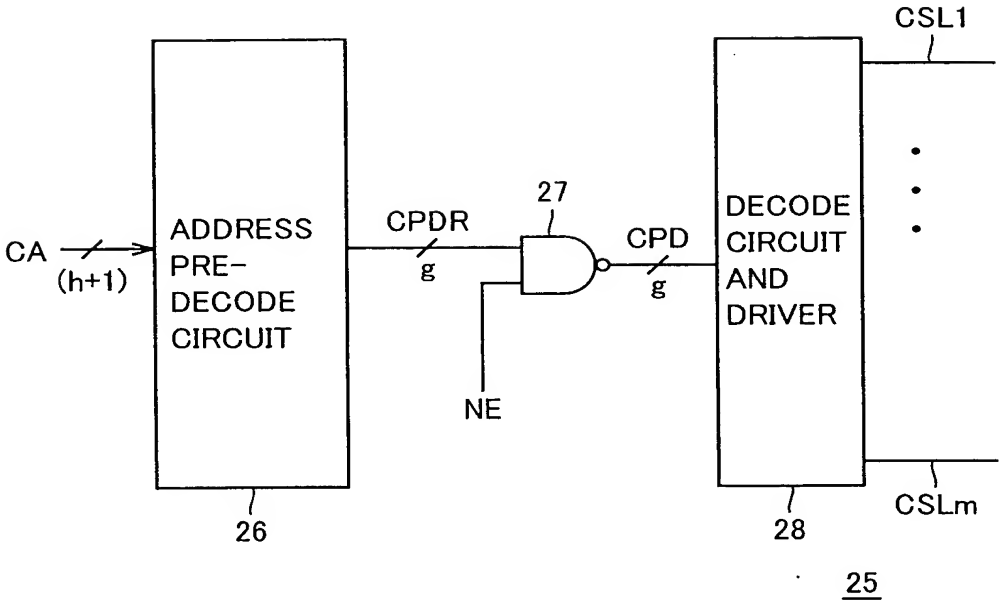

CSL1
CA
(h+1)
ADDRESS
PRE-
DECODE
CIRCUIT
CPDR
g
27
CPD
g
DECODE
CIRCUIT
AND
DRIVER
NE
CSLm
26
28
25

FIG.6

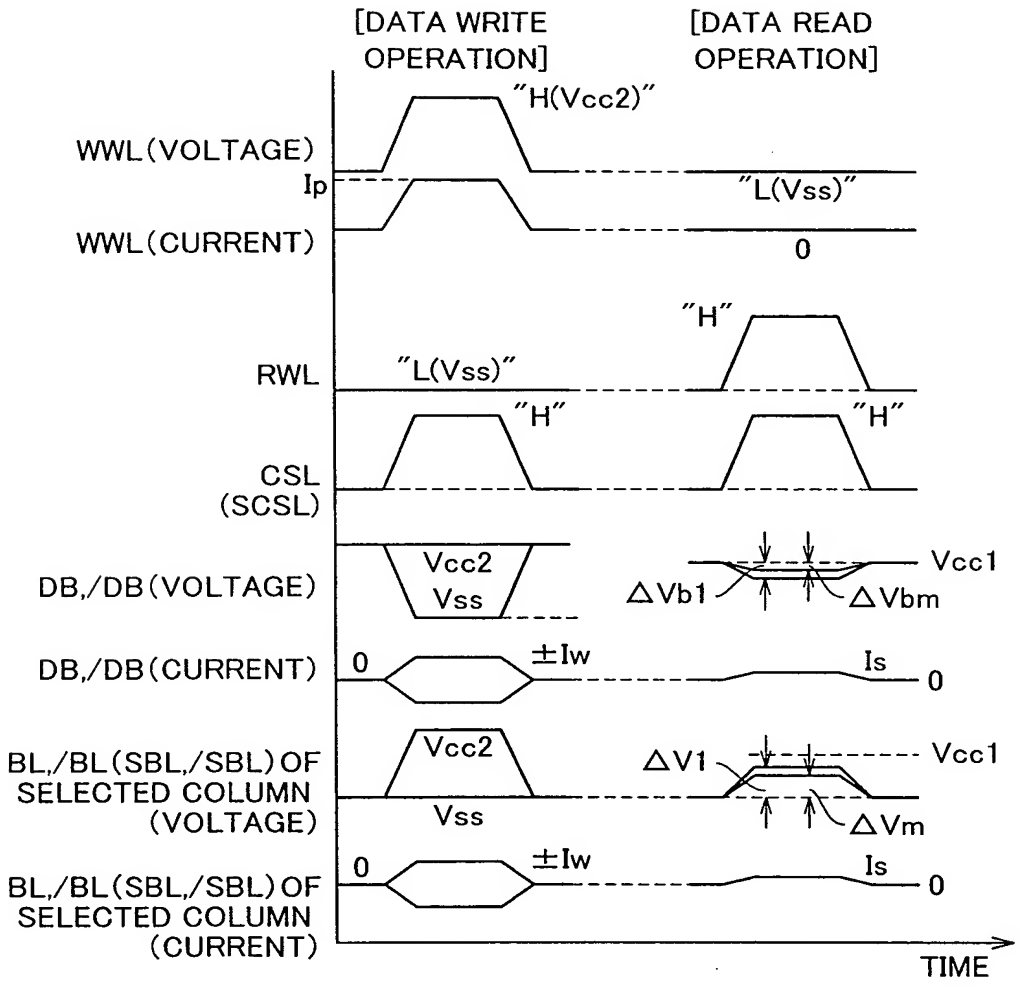

[DATA WRITE OPERATION]
[DATA READ OPERATION]
"H(Vcc2)"
WWL(VOLTAGE)
Ip
"L(Vss)"
WWL(CURRENT)
0
"H"
RWL
"L(Vss)"
"H"
"H"
CSL (SCSL)
Vcc2
Vss
Vcc1
DB,/DB(VOLTAGE)
ΔVb1
ΔVbm
0
±Iw
Is
0
DB,/DB(CURRENT)
Vcc2
ΔV1
Vcc1
BL,/BL(SBL,/SBL)OF SELECTED COLUMN (VOLTAGE)
Vss
ΔVm
0
±Iw
Is
0
BL,/BL(SBL,/SBL)OF SELECTED COLUMN (CURRENT)
TIME

FIG.7

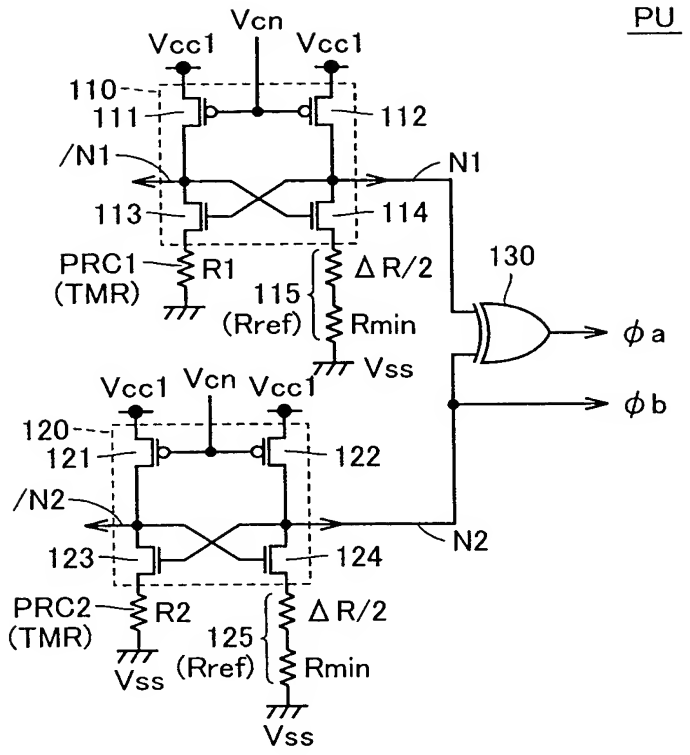


FIG.8

	INITIAL STATE	PROGRAM STATE 1	PROGRAM STATE 2	NON-PROGRAM STATE
PRC1(R1)	Rmin	Rmin	Rmax	(SAME AS INITIAL STATE)
PRC2(R2)	Rmin	Rmax	Rmin	(SAME AS INITIAL STATE)
OUTPUT φa	"L"	"H"	"H"	(SAME AS INITIAL STATE)
OUTPUT φb	"H"	"L"	"H"	(SAME AS INITIAL STATE)

FIG.9A

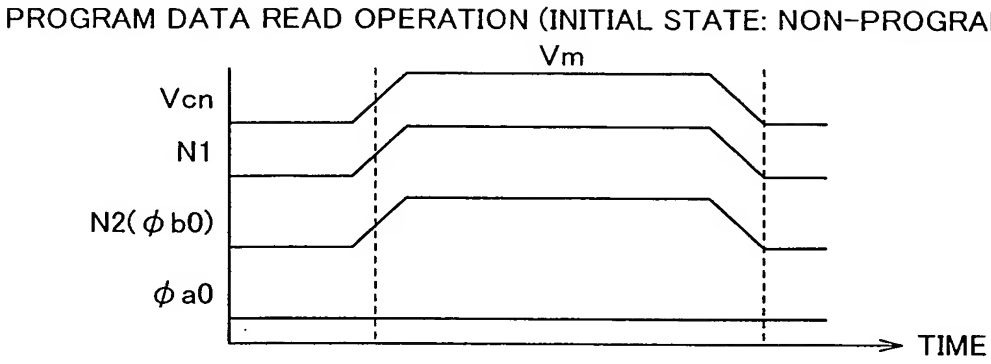


FIG.9B

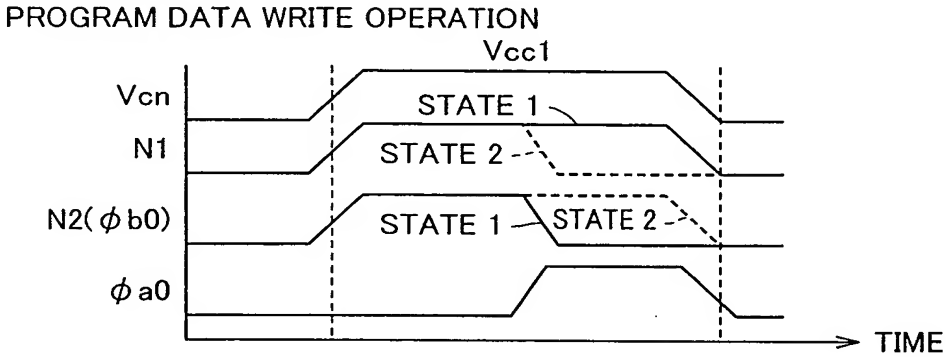


FIG.9C

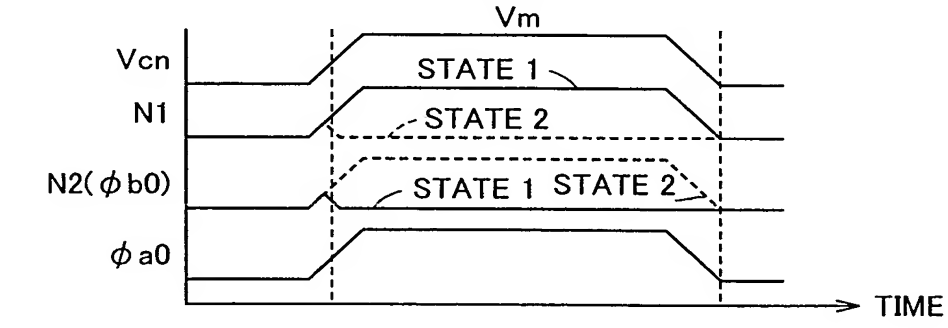


FIG.10

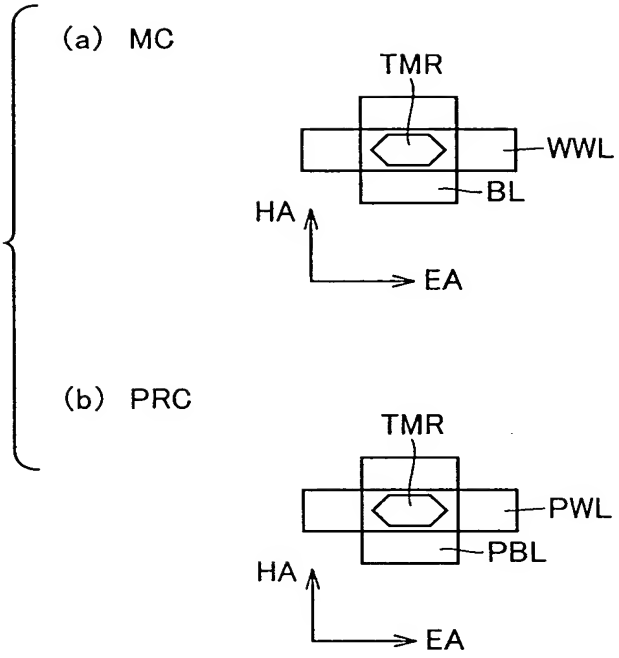


FIG.11A

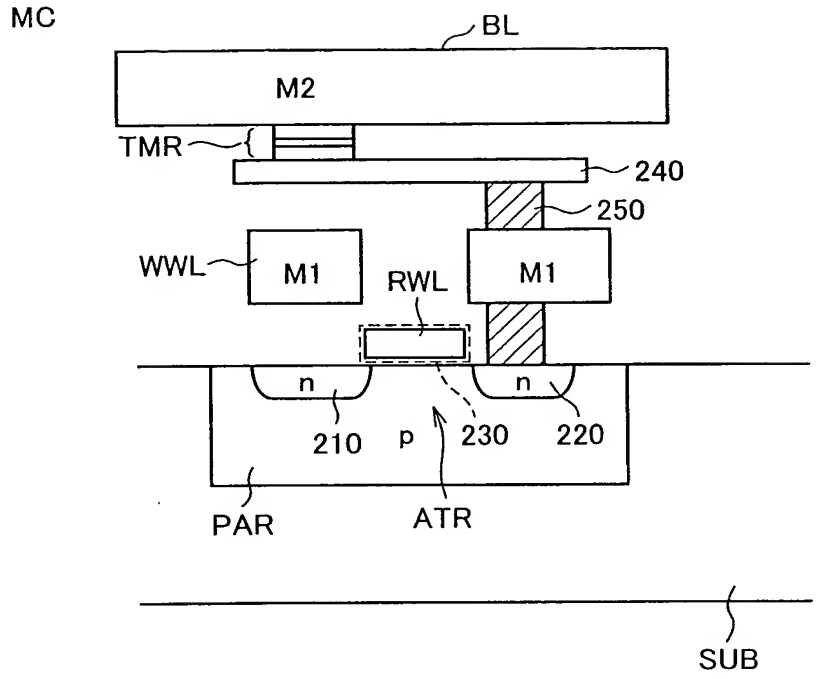
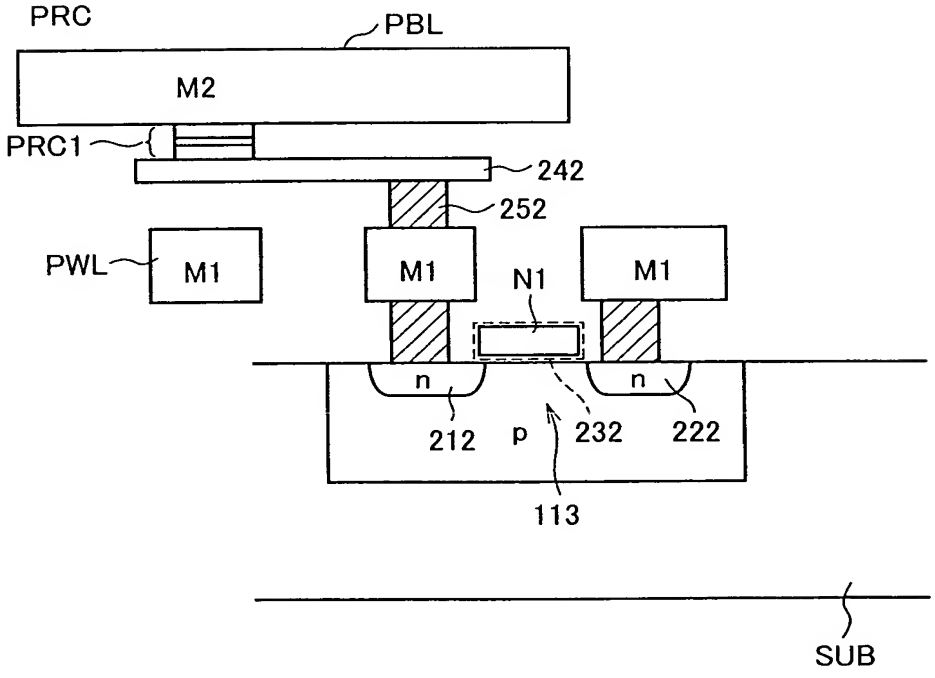


FIG.11B



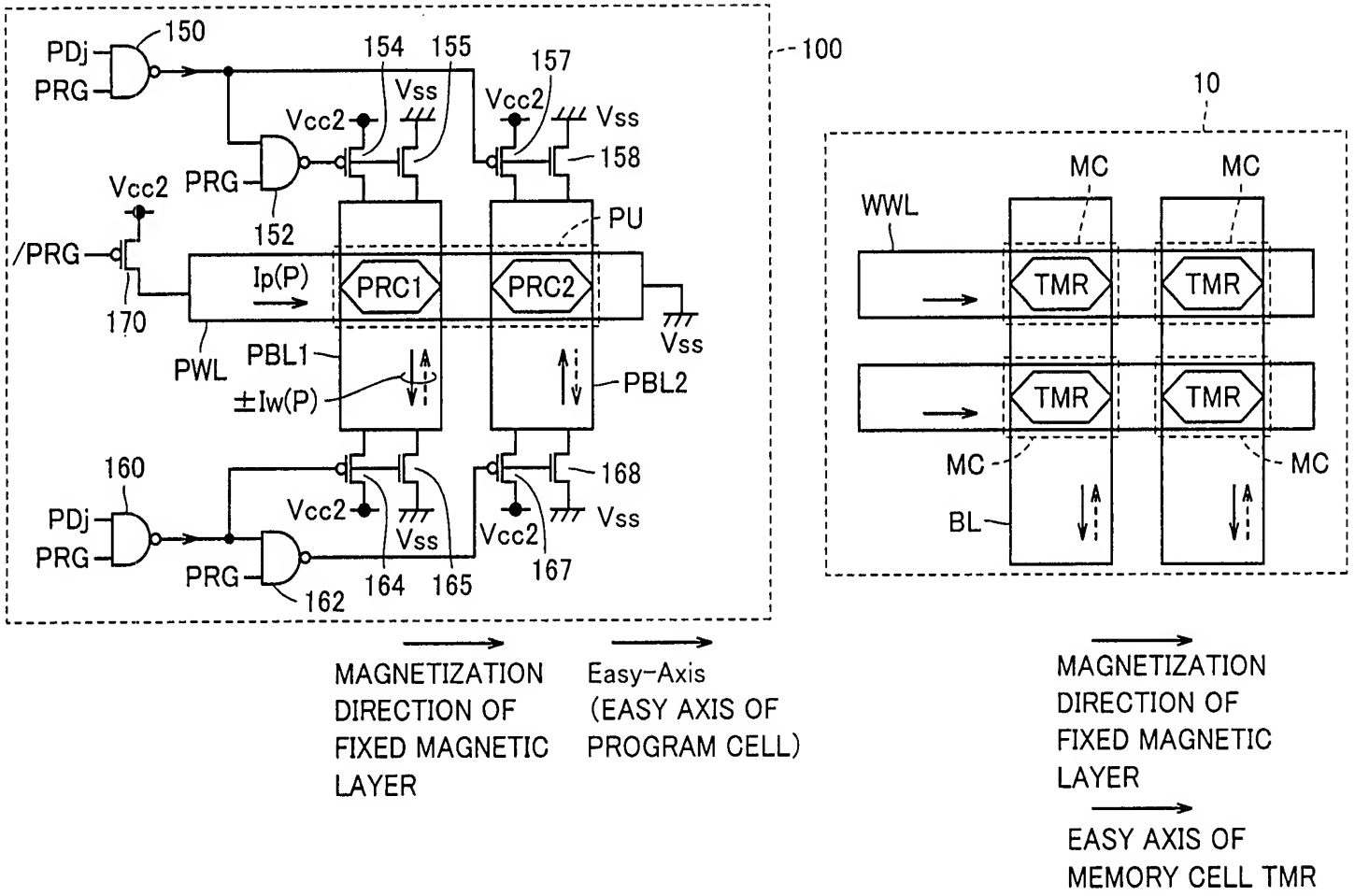

100
PDj
PRG
150
154
155
157
Vss
Vcc2
Vss
158
Vcc2
PRG
152
PU
/PRG
Ip(P)
PRC1
PRC2
170
Vss
PWL
PBL1
±Iw(P)
PBL2
160
168
Vcc2
Vss
Vcc2
Vss
PDj
PRG
PRG
162
164
165
167
MAGNETIZATION DIRECTION OF FIXED MAGNETIC LAYER
Easy-Axis (EASY AXIS OF PROGRAM CELL)
10
MC
MC
WWL
TMR
TMR
TMR
TMR
MC
MC
BL
MAGNETIZATION DIRECTION OF FIXED MAGNETIC LAYER
EASY AXIS OF MEMORY CELL TMR

FIG.12

FIG.13

	INITIAL STATE	PROGRAM STATE 1	PROGRAM STATE 2	NON-PROGRAM STATE
PDj	—	"L"	"H"	—
PRG	—	"H"	"H"	"L"
PRC1(R1)	Rmin	Rmin	Rmax	(SAME AS INITIAL STATE)
PRC2(R2)	Rmin	Rmax	Rmin	(SAME AS INITIAL STATE)
OUTPUT ϕ a	"L"	"H"	"H"	(SAME AS INITIAL STATE)
OUTPUT ϕ b	"H"	"L"	"H"	(SAME AS INITIAL STATE)

FIG.14

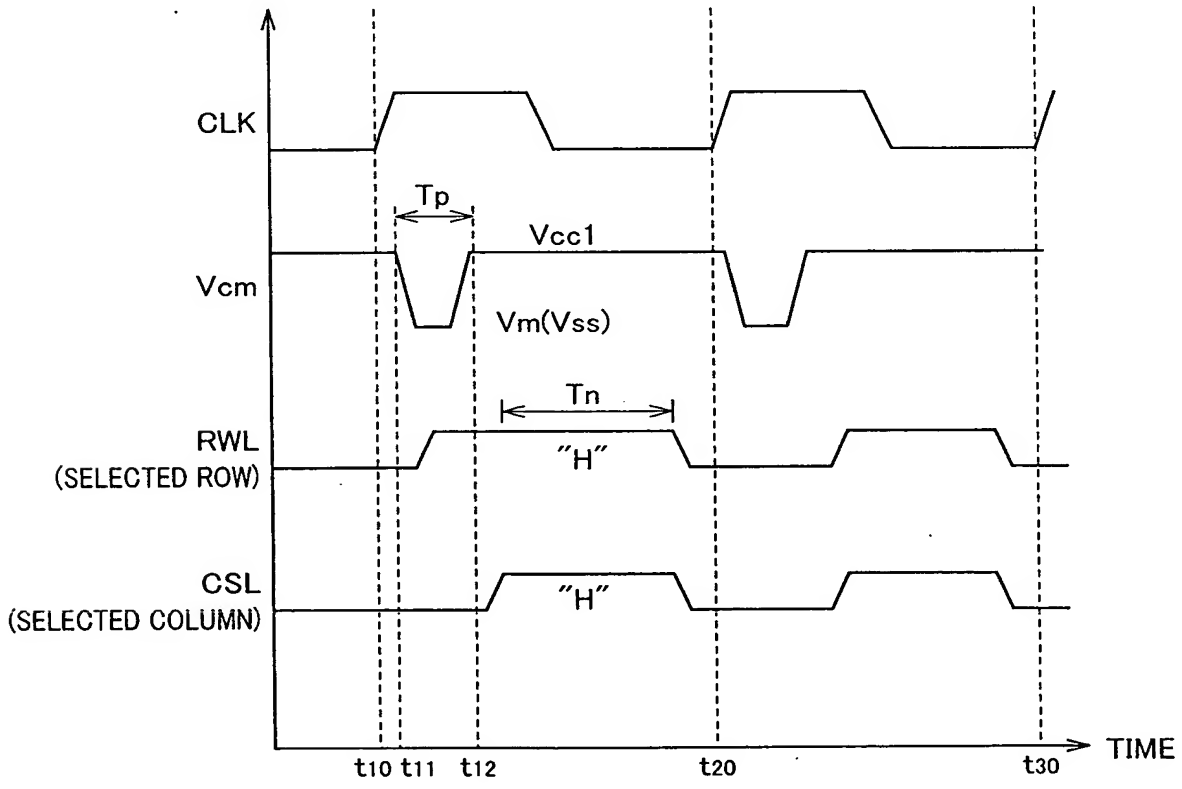


FIG.15

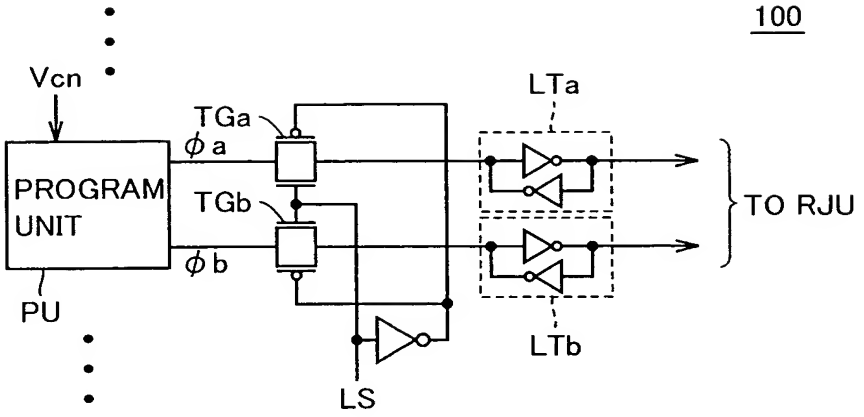

100
Vcn
PROGRAM UNIT
PU
TGa
φa
TGb
φb
LS
LTa
LTb
TO RJU

FIG.16

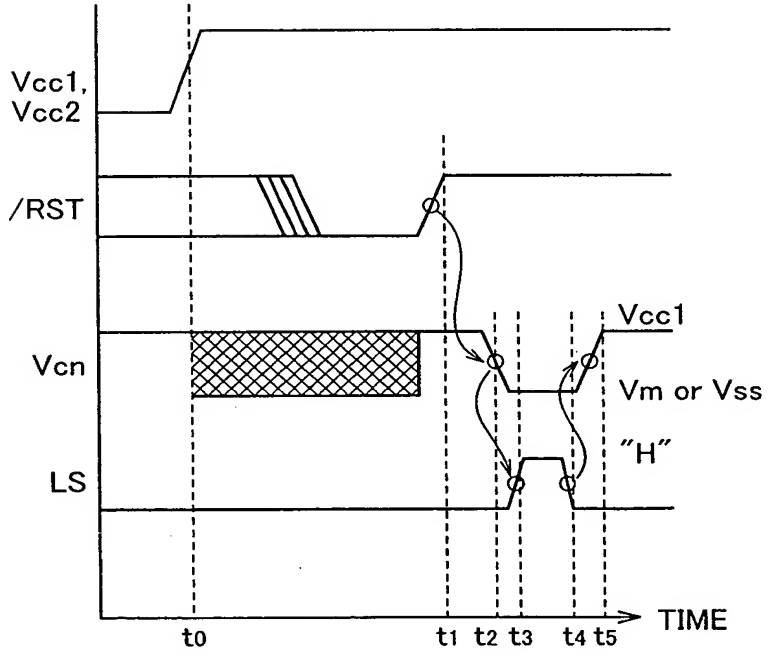

Vcc1, Vcc2
/RST
Vcn
LS
Vcc1
Vm or Vss
"H"
TIME
t0
t1
t2
t3
t4
t5

FIG.17

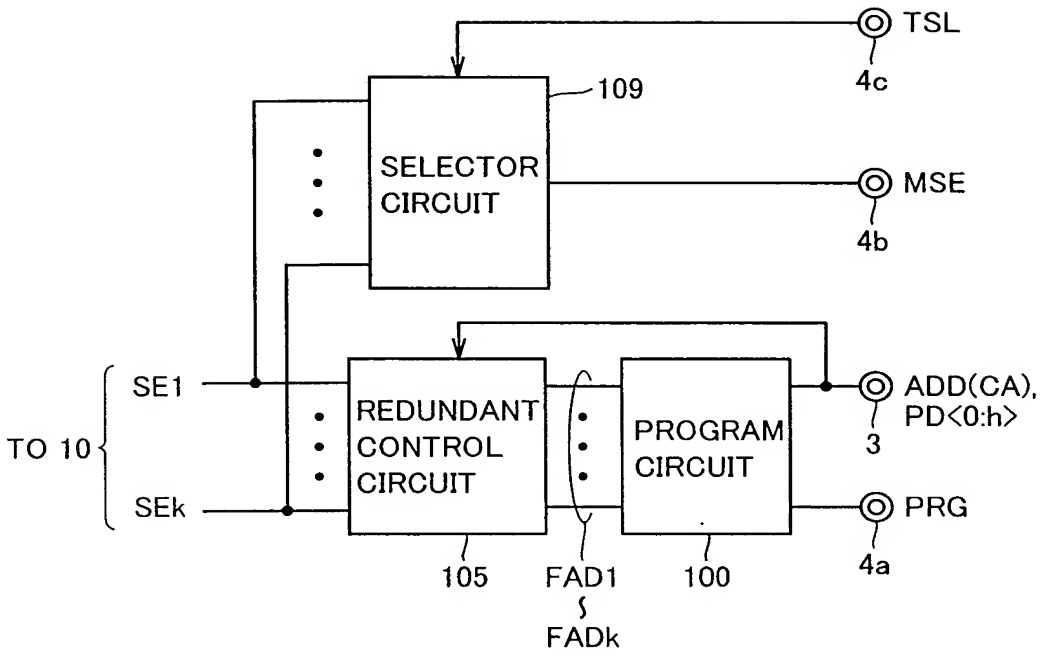

TSL
4c
109
SELECTOR CIRCUIT
MSE
4b
SE1
TO 10
SEk
REDUNDANT CONTROL CIRCUIT
PROGRAM CIRCUIT
ADD(CA), PD<0:h>
3
PRG
4a
105
FAD1
FADk
100

FIG.18

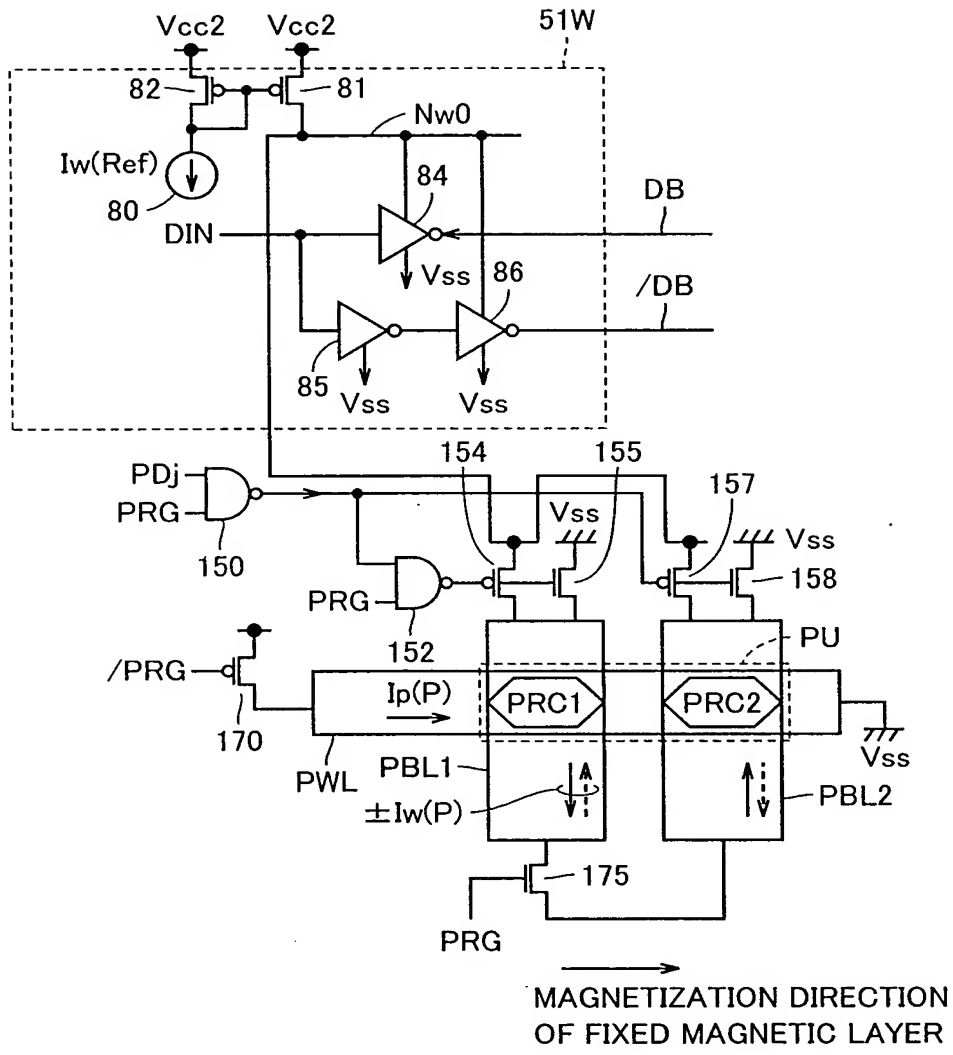

Vcc2
Vcc2
51W
82
81
Nw0
Iw(Ref)
80
84
DB
DIN
Vss
86
/DB
85
Vss
Vss
154
155
157
PDj
PRG
150
Vss
Vss
158
PRG
152
PU
/PRG
170
Ip(P)
PRC1
PRC2
Vss
PWL
PBL1
±Iw(P)
PBL2
175
PRG
MAGNETIZATION DIRECTION
OF FIXED MAGNETIC LAYER

FIG.19

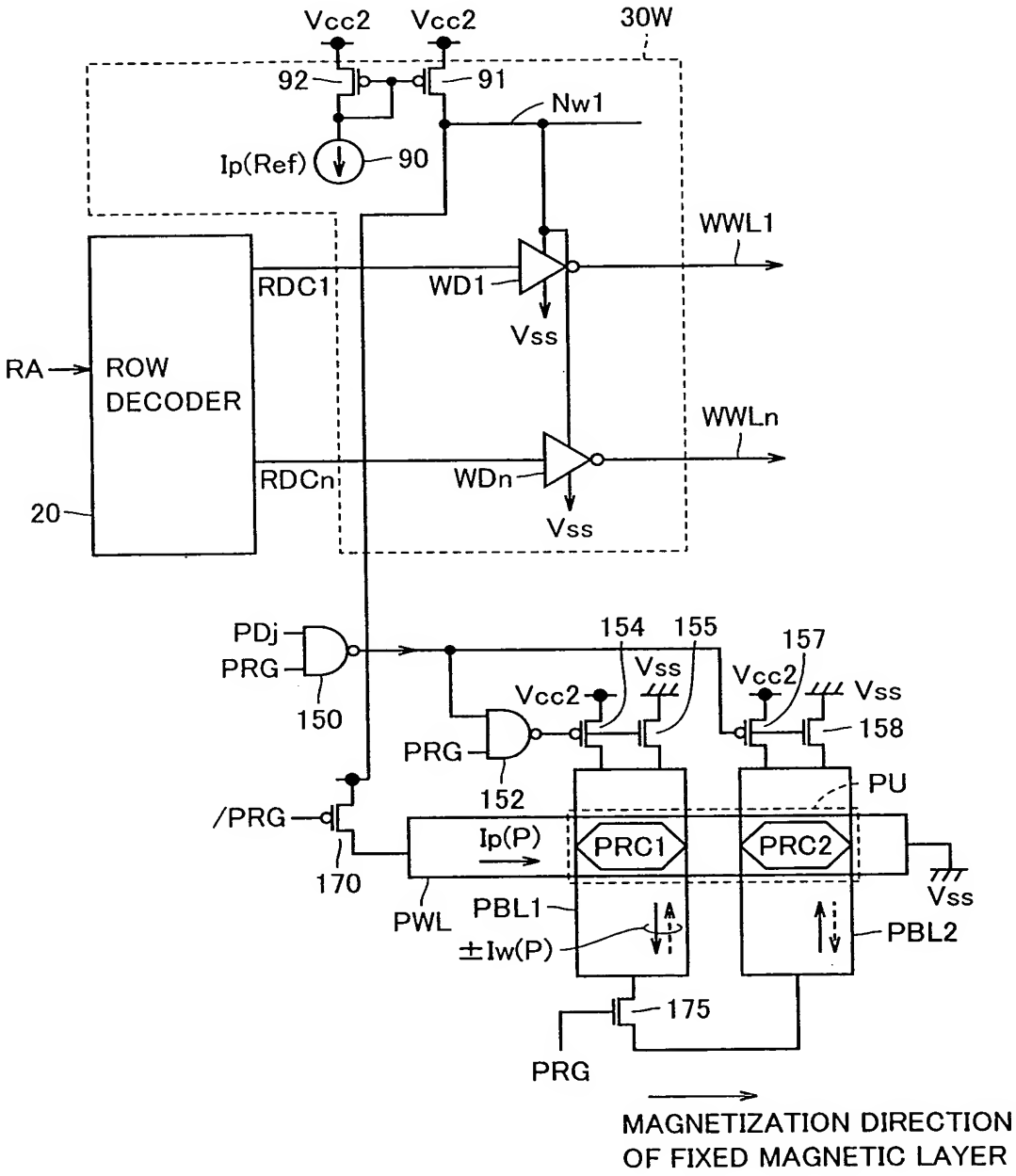

Vcc2
Vcc2
30W
92
91
Nw1
Ip(Ref)
90
WWL1
RDC1
WD1
Vss
RA
ROW
DECODER
WWLn
RDCn
WDn
20
Vss
PDj
PRG
150
154
155
157
Vss
Vcc2
Vcc2
Vss
158
PRG
152
PU
/PRG
Ip(P)
PRC1
PRC2
170
Vss
PWL
PBL1
±Iw(P)
PBL2
175
PRG
MAGNETIZATION DIRECTION
OF FIXED MAGNETIC LAYER

FIG.20

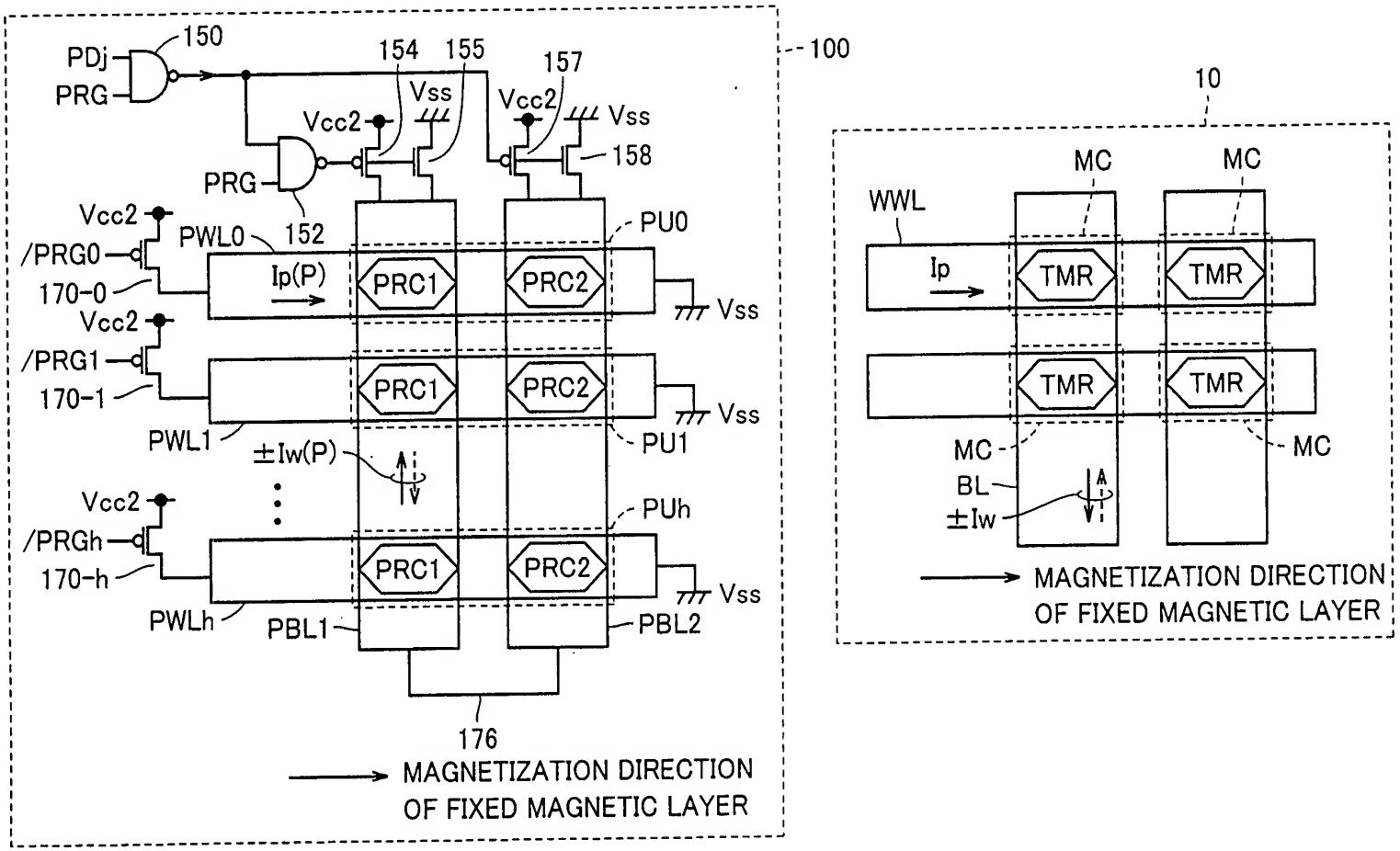

100
PDj
PRG
150
154
155
157
Vss
Vcc2
Vcc2
Vss
158
PRG
152
Vcc2
/PRG0
170-0
PWL0
Ip(P)
PRC1
PRC2
PU0
Vss
Vcc2
/PRG1
170-1
PRC1
PRC2
Vss
PWL1
±Iw(P)
PU1
Vcc2
/PRGh
170-h
PRC1
PRC2
PUh
Vss
PWLh
PBL1
PBL2
176
MAGNETIZATION DIRECTION
OF FIXED MAGNETIC LAYER
10
MC
MC
WWL
Ip
TMR
TMR
TMR
TMR
MC
MC
BL
±Iw
MAGNETIZATION DIRECTION
OF FIXED MAGNETIC LAYER

FIG.21

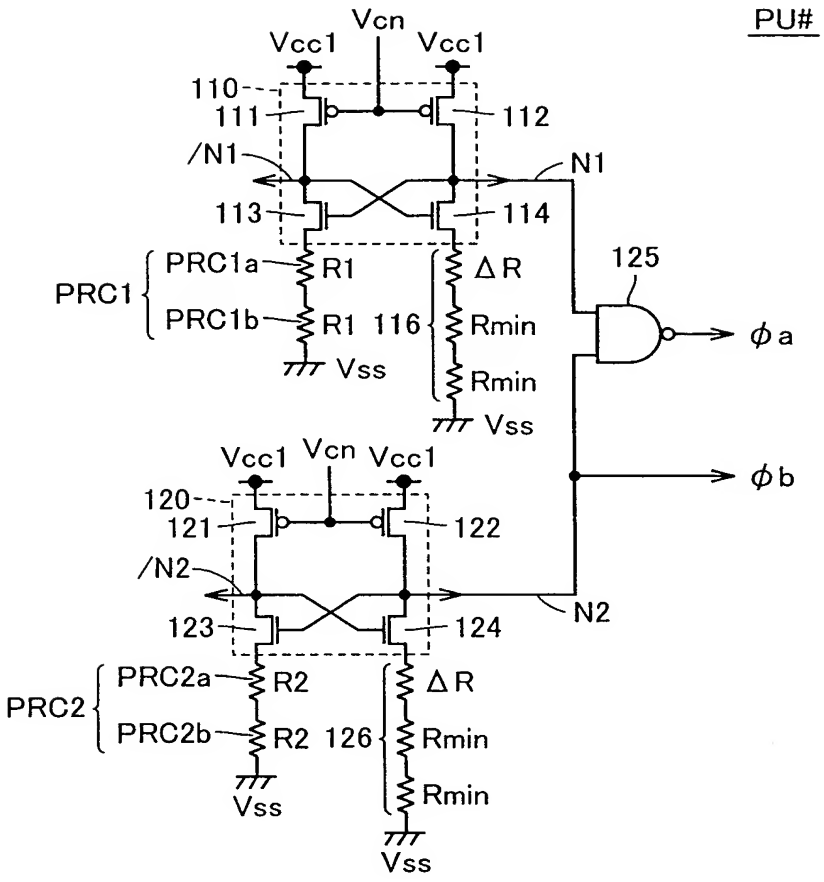

PU#
Vcn
Vcc1
Vcc1
110
111
112
/N1
N1
113
114
PRC1
PRC1a
R1
ΔR
125
PRC1b
R1
116
Rmin
φa
Vss
Rmin
Vss
Vcc1
Vcn
Vcc1
φb
120
121
122
/N2
N2
123
124
PRC2
PRC2a
R2
ΔR
PRC2b
R2
126
Rmin
Vss
Rmin
Vss

FIG.22

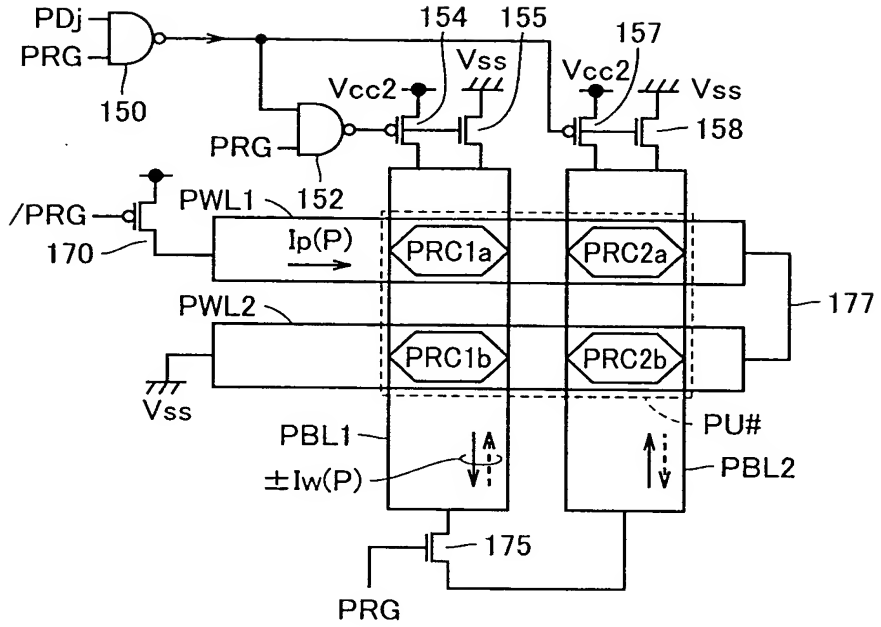

PDj
PRG
150
154
155
157
Vss
Vcc2
Vcc2
Vss
158
PRG
/PRG
170
PWL1
152
Ip(P)
PRC1a
PRC2a
177
PWL2
PRC1b
PRC2b
Vss
PU#
PBL1
±Iw(P)
PBL2
175
PRG

FIG.23

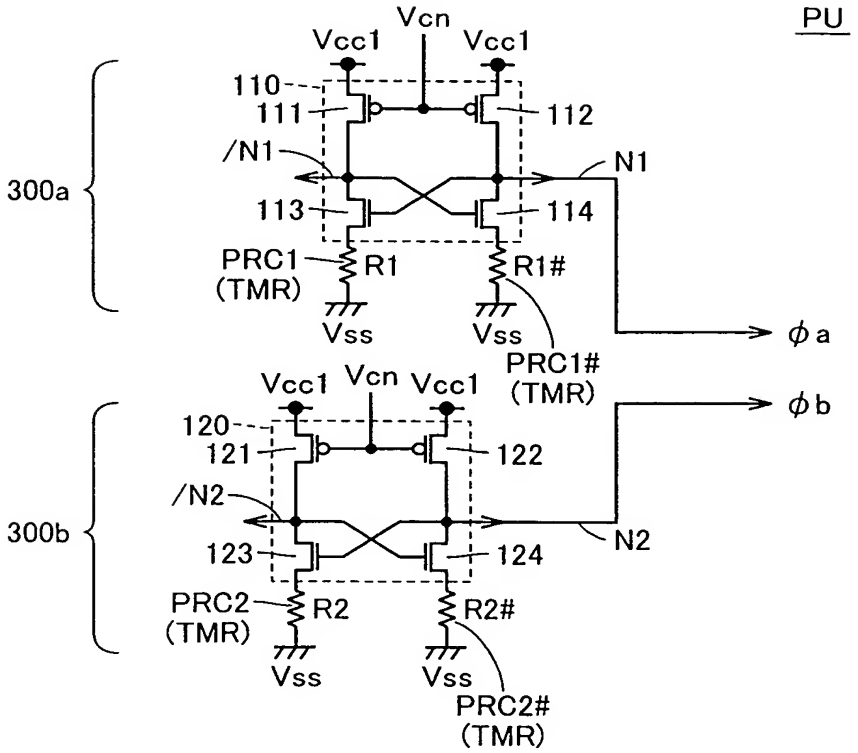


FIG.24

	INITIAL STATE	PROGRAM STATE 1	PROGRAM STATE 2	NON-PROGRAM STATE
PRC1(R1)	Rmax,Rmin	Rmin,Rmax	Rmin,Rmax	(SAME AS INITIAL STATE)
PRC2(R2)	Rmin,Rmin	Rmax,Rmin	Rmin,Rmax	(SAME AS INITIAL STATE)
OUTPUT ϕa	"L"	"H"	"H"	(SAME AS INITIAL STATE)
OUTPUT ϕb	– (INDETERMINATE)	"L"	"H"	(SAME AS INITIAL STATE)

FIG.25A

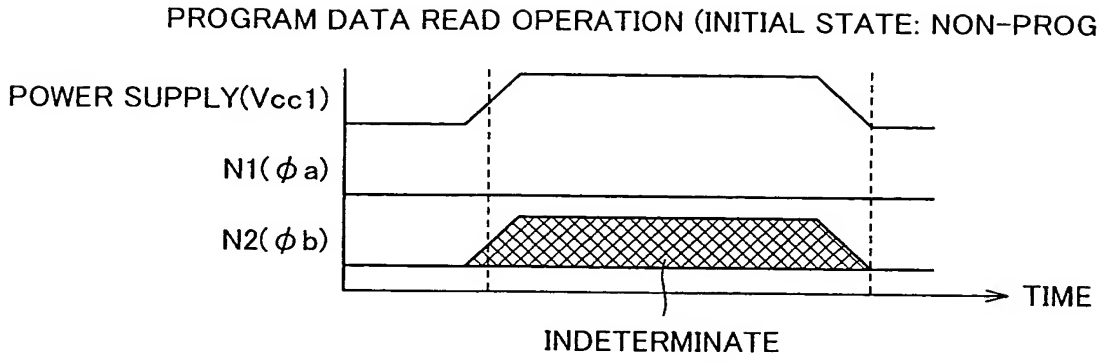


FIG.25B

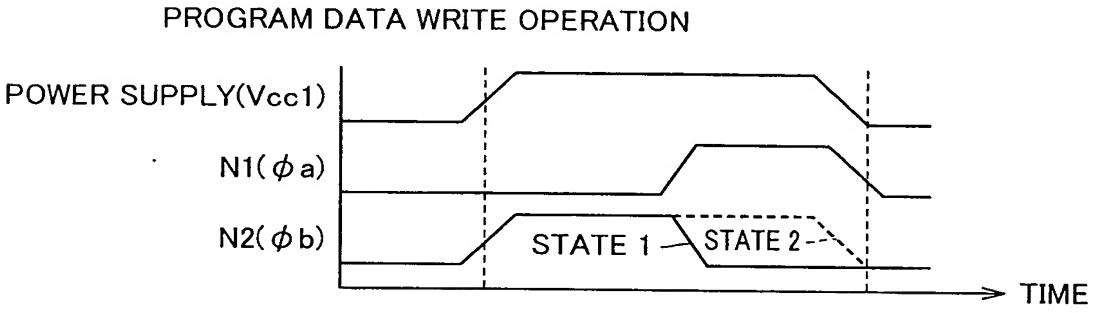
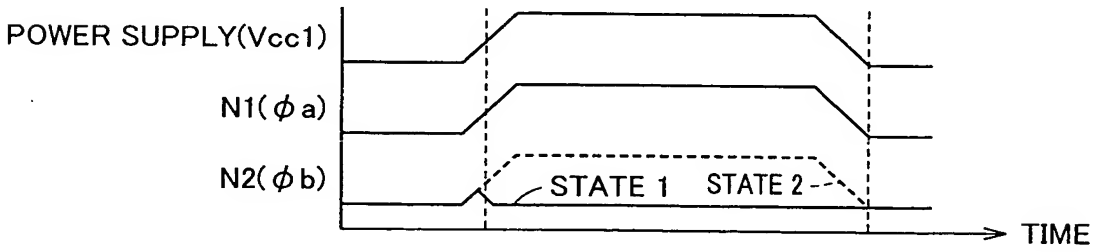


FIG.25C



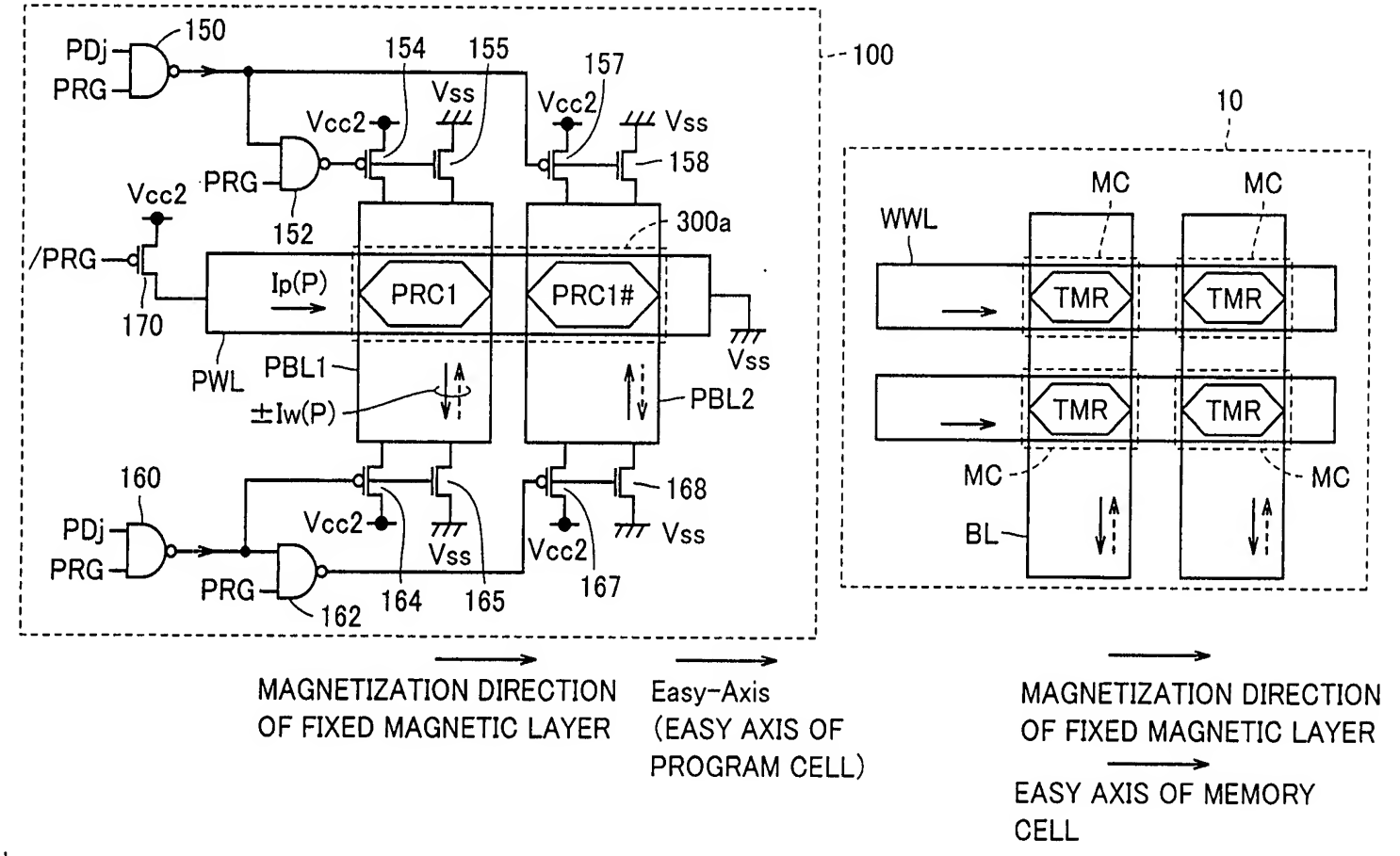

PDj
PRG
150
154
155
157
Vss
Vcc2
Vcc2
Vss
158
PRG
152
Vcc2
/PRG
170
300a
Ip(P)
PRC1
PRC1#
Vss
PWL
PBL1
±Iw(P)
PBL2
160
168
PDj
PRG
Vcc2
Vss
Vcc2
Vss
PRG
162
164
165
167
100
10
MC
MC
WWL
TMR
TMR
TMR
TMR
MC
MC
BL
MAGNETIZATION DIRECTION OF FIXED MAGNETIC LAYER
Easy-Axis (EASY AXIS OF PROGRAM CELL)
MAGNETIZATION DIRECTION OF FIXED MAGNETIC LAYER
EASY AXIS OF MEMORY CELL

FIG.26

FIG.27

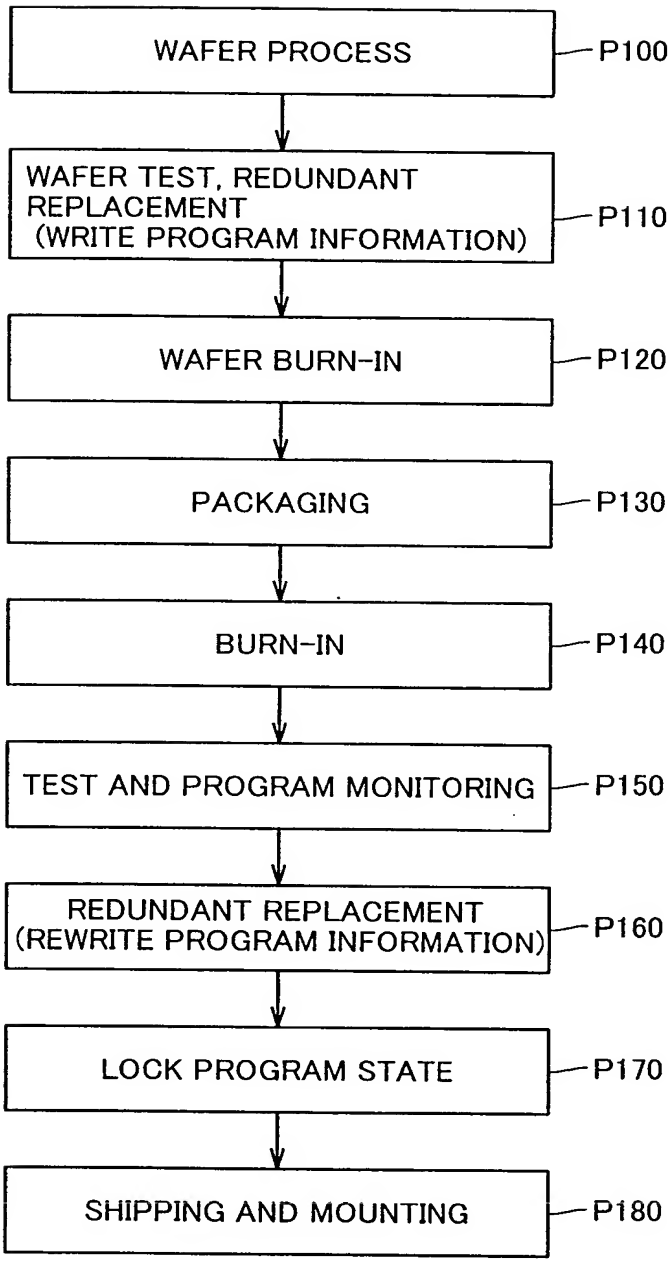

WAFER PROCESS
P100
WAFER TEST, REDUNDANT REPLACEMENT (WRITE PROGRAM INFORMATION)
P110
WAFER BURN-IN
P120
PACKAGING
P130
BURN-IN
P140
TEST AND PROGRAM MONITORING
P150
REDUNDANT REPLACEMENT (REWRITE PROGRAM INFORMATION)
P160
LOCK PROGRAM STATE
P170
SHIPPING AND MOUNTING
P180

FIG.28

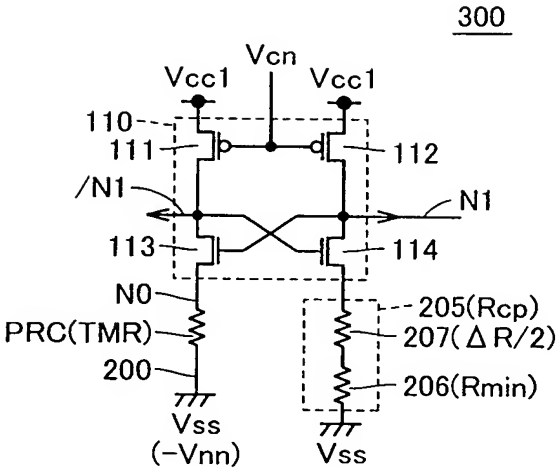


FIG.29A

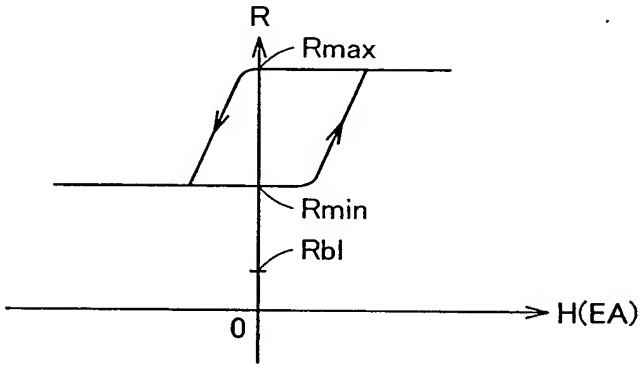


FIG.29B

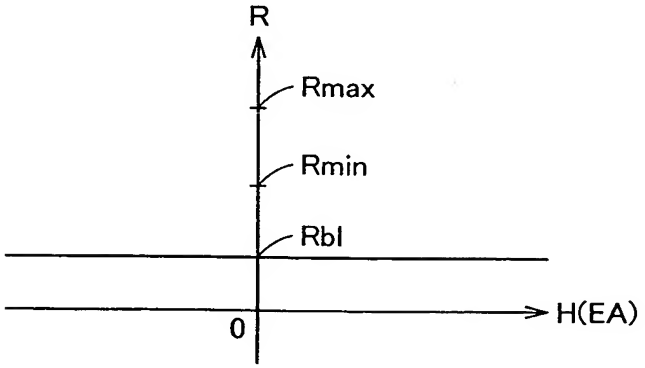


FIG.30

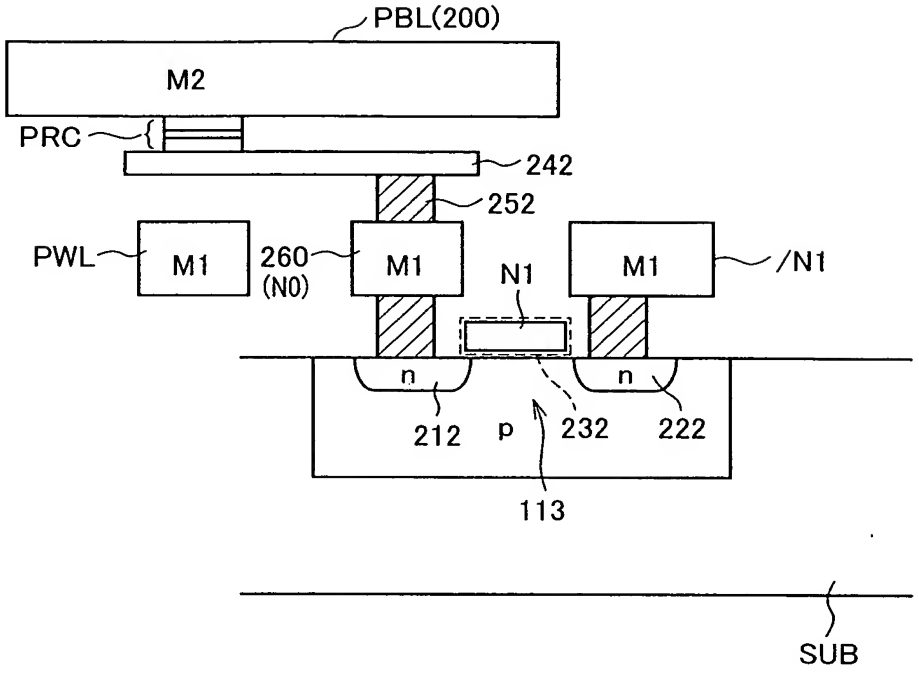

PBL(200)
M2
PRC
242
252
PWL
M1
260
(N0)
M1
N1
M1
/N1
n
n
212
p
232
222
113
SUB

FIG.31 PRIOR ART

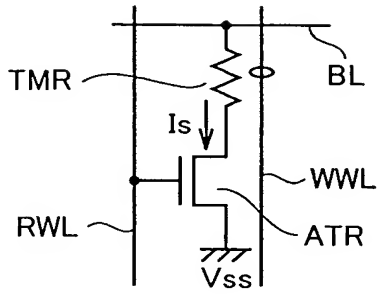


FIG.32 PRIOR ART

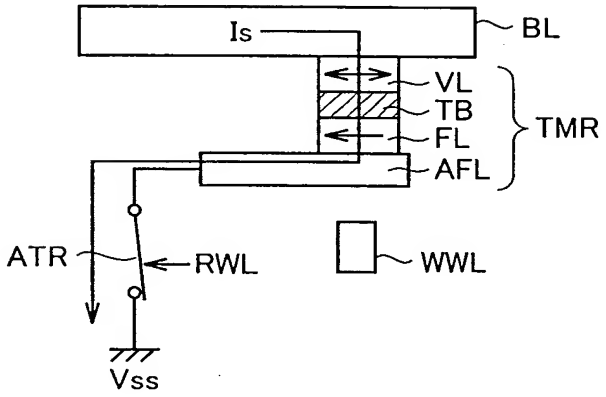


FIG.33 PRIOR ART

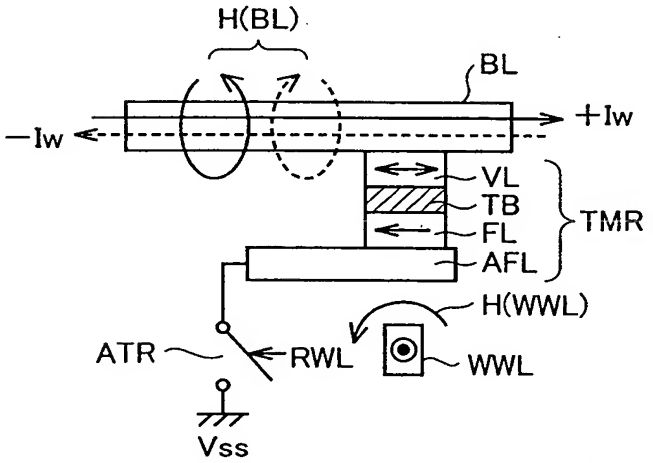


FIG.34 PRIOR ART